CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a silicon-on-insulator substrate structure comprising:

providing a graded porous Si-containing structure; and

oxidizing said graded porous Si-containing structure to form a silicon-on-insulator (SOI) structure having a uniform buried oxide layer and a Si-containing over-layer.

2. The method of Claim 1 wherein the providing step comprises ion implanting a dopant into a Si-containing substrate, activating the dopant within the Si-containing substrate to form an implanted and activated doped region and then subjecting said implanted and activated doped region to an electrolytic anodization process.

3. The method of Claim 2 wherein the dopant is an n-type dopant or a p-type dopant.

4. The method of Claim 3 wherein the dopant is a p-type dopant selected from the group consisting of Ga, Al, B and BF_2.

5. The method of Claim 4 wherein the p-type dopant is B, said B is implanted at an energy of from about 100 keV to about 500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

6. The method of Claim 4 wherein the p-type dopant is BF_2, said BF_2 is implanted at an energy of from about 500 keV to about 2500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

7. The method of Claim 2 wherein the activating step comprises annealing.

8. The method of Claim 7 wherein the annealing is selected from the group consisting of a furnace anneal, a rapid thermal anneal, and a spike anneal.

9. The method of Claim 8 wherein the annealing is a furnace anneal step, said furnace anneal step is carried out at a temperature of about 600°C or greater for a time period of about 15 minutes or greater in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

10. The method of Claim 8 wherein the annealing is a rapid thermal anneal (RTA) step, said RTA step is carried out at a temperature of about 800°C or greater for a time period of about 5 minutes or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

11. The method of Claim 8 wherein the annealing is a spike annealing step, said spike annealing step is performed at a temperature of about 900°C or greater for a time period of about 1 second or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

12. The method of Claim 2 wherein the anodization process is performed in the presence of a HF-containing solution.

13. The method of Claim 12 wherein the anodization process is performed using a constant current source operating at a current density of from about 0.05 to about 50 milliAmps/cm^2.

14. The method of Claim 1 wherein the porous Si-containing region has a porosity of about 0.01% or greater.

15. The method of Claim 1 wherein the porous Si-containing region comprises an upper region of less dense porous Si and a lower region of more dense porous Si.

16. The method of Claim 1 further comprising forming a cap layer atop the Si-containing substrate after said providing step, but prior to said oxidizing.

17. The method of Claim 16 wherein the cap layer comprises a Si-containing material.

18. The method of Claim 1 wherein the oxidizing is performed in an oxygen-containing ambient.

19. The method of Claim 18 wherein the oxygen-containing ambient further comprises an inert gas.

20. The method of Claim 19 wherein the oxygen-containing ambient is selected from the group consisting of O_2, NO, N_2O, ozone, and air.

21. The method of Claim 1 wherein the oxidizing is performed at a temperature of from about 650°C to about 1350°C.

22. The method of Claim 1 wherein the oxidizing forms a surface oxide atop the Si-containing over-layer.

23. The method of Claim 1 wherein the porous Si-containing region is continuous.

24. The method of Claim 1 wherein the porous Si-containing region comprises discrete islands and said buried oxide of said SOI structure comprises discrete islands of thermal oxide.

25. The method of Claim 24 wherein the discrete islands of porous Si and buried oxide are consumed.

26. The method of Claim 1 further comprising repeating the providing and oxidizing steps any number of times to provide a multi-layered Si-on-insulator material.

27. The method of Claim 1 further comprising a pre-oxidization step prior to said oxidizing, said pre-oxidization step includes oxidation in a wet oxygen ambient.

28. The method of Claim 27 wherein said pre-oxidization step is performed at a temperature from about 600°C to about 1200°C.

29. The method of Claim 1 further comprising a post oxidation step, said post oxidation step comprising a thermal anneal in a hydrogen ambient.

30. The method of Claim 29 wherein the post oxidization step is performed at a temperature from about 900°C to about 1200°C.

31. The method of Claim 2 further comprising implanting a neutral ion into said Si-containing substrate prior to or after said implanting of said dopant.

32. The method of Claim 31 wherein said neutral ion comprises Si, Ne, Sn, Bi or Xe.

33. The method of Claim 31 wherein said implanting of neutral ions forms an amorphized region in said Si-containing substrate.

34. The method of Claim 31 wherein said neutral ion is Si and said implanting step is performed using a Si dose from about 1E15 to about 1E16 atoms/cm^2 and an implant energy from about 200 to about 500 keV at or below nominal room temperature.

35. The method of Claim 1 wherein said oxidizing step is performed using conditions sufficient to form a broken buried oxide region and a continuous buried oxide region.

36. The method of Claim 35 wherein said oxidizing is performed at a temperature below 1000°C.

37. A method of fabricating a Si-on-insulator comprising:

providing a structure containing an implanted and activated dopant region within a Si-containing substrate;

converting the doped region into a graded porous Si-containing region by an HF anodization process;

subjecting the structure containing the graded porous Si-containing region to a thermal wet oxidation process;

oxidizing the structure containing the porous Si-containing region to form a silicon-on-insulator (SOI) structure having a uniform buried oxide layer and a Si-containing over-layer; and

subjecting said SOI structure to a post oxidation thermal anneal which is carried out in a hydrogen ambient.

38. A method of forming a patterned Si-on-insulator comprising

providing a patterned graded porous Si-containing structure; and

oxidizing said patterned graded porous Si-containing structure to form a silicon-on-insulator (SOI) structure having a uniform buried oxide layer and a Si-containing over-layer.